

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1 Claim 1 (currently amended): A bi-directional communication  
2 link having plural channels, each of said channels  
3 comprising:  
4 | a master connected at a near end of the channel and a  
5 slave connected at an opposite end of the channel;  
6 said master comprising:  
7 (a) a transmitter coupled to the channel and  
8 | having a master Tx clock signal; and  
9 (b) a receiver coupled to the channel and  
10 comprising:  
11 (i) an analog-to-digital converter that  
12 periodically samples at a sampling time  $T_s$ ;  
13 (ii) a clock recovery circuit that generates  
14 a master Rx clock from a clock signal embedded in a signal  
15 | received from the channel; and  
16 (iii) a metric processor connected to an  
17 output of said analog-to-digital converter that produces a  
18 metric signal ~~indicative of resolution~~ reflective of  
19 amplitude differences between the received signal and allowed  
20 amplitude levels of the received signal; and  
21 said slave comprising:  
22 (a) a receiver coupled to the channel and  
23 comprising a clock recovery circuit for generating a Slave Rx  
24 clock from the signal received from the master;

25 (b) a transmitter coupled to the channel and  
26 having a Slave Tx clock signal, whereby said master Rx clock  
27 signal is frequency locked to said Slave Tx clock signal; and

28 (c) a first controllable delay element for  
29 generating said Slave Tx clock signal from said Slave Rx  
30 clock signal; and

31 said communication link further comprising a  
32 decision processor responsive to said metric processor for  
33 changing a delay value of said controllable delay element so  
34 as to maximize the metric signal.

Claims 2-3 (canceled)

1 Claim 4 (original): The apparatus of claim 1 further  
2 comprising a second controllable delay between said Master Rx  
3 clock signal and said analog-to-digital converter and  
4 responsive to said decision processor, whereby said decision  
5 processor delays the Slave Tx clock signal and the sample  
6 time Ts independently to maximize the metric signal.

1 Claim 5 (currently amended): A bi-directional communication  
2 link having plural channels with respective masters and  
3 slaves at respective ends of respective channels, each master  
4 issuing a Master Tx clock, each slave constructing a Slave Rx  
5 clock frequency-locked to the Master Tx clock, and a Slave Tx  
6 clock frequency-locked to the Slave Rx clock, said  
7 bi-directional communication link comprising:

8 a metric processor for each master that produces a  
9 metric signal indicative of resolution reflective of  
10 amplitude differences between a signal received by the master  
11 from the corresponding slave and allowed amplitude levels of  
12 the received signal; and

13           a decision processor responsive to said metric  
14 processor for changing the phase of the Slave Tx clock  
15 relative to the Slave Rx clock so as to maximize the metric  
16 signal.

Claims 6-7 (canceled)

1    Claim 8 (currently amended): A bi-directional communication  
2    link having plural channels with respective masters and  
3    slaves at respective ends of respective channels, each master  
4    issuing a Master Tx clock, each slave constructing a Slave Rx  
5    clock frequency-locked to the Master Tx clock, and a Slave Tx  
6    clock frequency-locked to the Slave Rx clock, wherein the  
7    master samples a signal it receives from the slave at a  
8    sample time  $T_s$  frequency locked to the Master Rx clock, said  
9    bi-directional communication link comprising:

10           a metric processor for each master that produces a  
11    metric signal indicative of resolution reflective of  
12    amplitude differences between a signal received by the master  
13    from the corresponding slave and allowed amplitude levels of  
14    the received signal; and

15           a decision processor responsive to said metric  
16 processor for shifting said sample time  $T_s$  relative to the  
17 Master Tx clock so as to maximize the metric signal.

Claims 9-10 (canceled)

1    Claim 11 (currently amended): A bi-directional communication  
2    link having plural channels with respective masters and  
3    slaves at respective ends of respective channels, each master  
4    issuing a Master Tx clock, each slave constructing a Slave Rx  
5    clock frequency-locked to the Master Tx clock, and a Slave Tx

6 clock frequency-locked to the Slave Rx clock, wherein each  
7 master receives a periodic noise burst comprising cross-talk  
8 from masters of adjacent channels and echoes of itself, ~~said~~  
9 ~~noise capable of reducing the resolution of a signal received~~  
10 ~~by the master from the slave over the corresponding~~  
11 ~~communication,~~ said bi-directional communication link  
12 comprising:

13 a metric processor for each master that produces a  
14 metric signal ~~indicative of the resolution~~ reflective of  
15 amplitude differences between of the signal received by the  
16 master from the corresponding slave and allowed amplitude  
17 levels of the received signal; and

18 a decision processor responsive to said metric  
19 processor for changing the phase of the Slave Tx clock  
20 relative to the Slave Rx clock so as to reduce the effects of  
21 the noise burst on the received signal and thereby increase  
22 the metric signal.

Claims 12-13 (canceled)

1 Claim 14 (currently amended): A bi-directional communication  
2 link having plural channels with respective masters and  
3 slaves at respective ends of respective channels, each master  
4 issuing a Master Tx clock, each slave constructing a Slave Rx  
5 clock frequency-locked to the Master Tx clock, and a Slave Tx  
6 clock frequency-locked to the Slave Rx clock, wherein the  
7 master samples a signal it receives from the slave at a  
8 sample time  $T_s$  frequency locked to the Master Rx clock, and  
9 wherein each master receives a periodic noise burst  
10 comprising cross-talk from masters of adjacent channels and  
11 echoes of itself, ~~said noise capable of reducing the~~  
12 ~~resolution of a signal received by the master from the slave~~

13 | ~~over the corresponding communication,~~ said bi-directional  
14 | communication link comprising:

15 |       a metric processor for each master that produces a  
16 | metric signal ~~indicative of the resolution~~ reflective of  
17 | amplitude differences between the signal received by the  
18 | master from the corresponding slave and allowed amplitude  
19 | levels of the received signal; and

20 |       a decision processor responsive to said metric  
21 | processor for shifting said sample time  $T_s$  relative to the  
22 | Master Tx clock so as to reduce the effects of the noise  
23 | burst on the received signal and thereby increase the metric  
24 | signal.

Claims 15-18 (canceled)

1 | Claim 19 (currently amended): The apparatus of claim ~~16-14~~  
2 | wherein said metric processor comprises a processor for  
3 | computing the proportion of samples of the signal received by  
4 | ~~the said each~~ master falling within allowed amplitude levels  
5 | relative to those that fall outside of said allowed amplitude  
6 | levels.

1 | Claim 20 (currently amended): In a bi-directional  
2 | communication link having plural channels with respective  
3 | masters and slaves at respective ends of respective channels,  
4 | each master issuing a Master Tx clock, each slave  
5 | constructing a Slave Rx clock frequency-locked to the Master  
6 | Tx clock, and a Slave Tx clock frequency-locked to the Slave  
7 | Rx clock, wherein the master samples a signal it receives  
8 | from the slave at a sample time  $T_s$  frequency locked to the  
9 | Master Rx clock, and wherein each master receives a periodic  
10 | noise burst comprising cross-talk from masters of adjacent

11 | channels and echoes of itself, ~~said noise capable of reducing~~  
12 | ~~the resolution of a signal received by the master from the~~  
13 | ~~slave over the corresponding communication,~~ a method of  
14 | reducing the effects of the cross-talk and echo noise burst  
15 | on the signal received by each master, comprising:

16 |       for said each master, producing a metric signal  
17 | ~~indicative of the resolution~~ reflective of amplitude  
18 | differences between the signal received by the master from  
19 | the corresponding slave and allowed amplitude levels of the  
20 | received signal; and

21 |       in response to said metric signal, shifting said sample  
22 | time  $T_s$  relative to the Master Tx clock so as to reduce the  
23 | effects of the noise burst on the received signal and thereby  
24 | increase the metric signal.

Claims 21-22 (canceled)

1 | Claim 23 (currently amended): The method of claim 20 wherein  
2 | the shifting of ~~said sample time  $T_s$~~  is carried out by step  
3 | comprises the step of changing a delay between said Slave Rx  
4 | clock and said Slave Tx clock.

Claim 24 (canceled)

1 | Claim 25 (currently amended): The method of claim ~~22~~ 20  
2 | wherein the producing of ~~the metric signal~~ step comprises the  
3 | step of computing ~~the~~ a proportion of samples of the signal  
4 | received by ~~the~~ said each master falling within the allowed  
5 | amplitude levels relative to those that fall outside of the  
6 | allowed amplitude levels.

Claim 26 (canceled)

1 Claim 27 (new): The apparatus of claim 1 wherein said metric  
2 processor comprises a processor for computing the proportion  
3 of samples of the signal received by the master falling  
4 within the allowed amplitude levels relative to those that  
5 fall outside of the allowed amplitude levels.

1 Claim 28 (new): The apparatus of claim 5 wherein said metric  
2 processor comprises a processor for computing the proportion  
3 of samples of the signal received by said each master falling  
4 within the allowed amplitude levels relative to those that  
5 fall outside of the allowed amplitude levels.

1 Claim 29 (new): The apparatus of claim 8 wherein said metric  
2 processor comprises a processor for computing the proportion  
3 of samples of the signal received by said each master falling  
4 within the allowed amplitude levels relative to those that  
5 fall outside of the allowed amplitude levels.

1 Claim 30 (new): The apparatus of claim 11 wherein said metric  
2 processor comprises a processor for computing the proportion  
3 of samples of the signal received by said each master falling  
4 within the allowed amplitude levels relative to those that  
5 fall outside of the allowed amplitude levels.